OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	09145.0008	Appln. No.	09/347,106
Applicant	Stanley A. HRONIK		
Filing Date	July 2, 1999	Group:	2186

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MM	Nakamura, Kazuyuki et al., *SP 24.6: A 500MHz 4Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O*, 1997 IEEE International Solid State Circuits Conference, Digest of Technical Papers, First Edition, February 1997, pp. 406-407.

Examiner	MM	Date Considered	12/5/03

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 — Patent and Trademark Office - U.S. Department of Commerce